Amendments to the Claims:

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1.-14. (Cancelled)

Claim 15. (New) A method for automatically allocating addresses among control devices connected to a data bus system, in which the control devices interchange data, using respective transmission/reception units, via a common data bus line, and simultaneously access data sent using the common data bus line; said method comprising:

starting an address allocation period by transmitting a message on the common data bus line to a plurality of control devices that are to be addressed;

in response to the message, during the address allocation period, electrically breaking the common data bus line into individual subsections, by each of the control devices which are to be addressed using a respective isolating means for electrically breaking the common data bus line; and

each of the control devices which are to be addressed placing its respective transmission/reception unit at a transmission potential.

Claim 16. (New) The method as claimed in Claim 15, wherein, during a period of address allocation:

each control device has an individually assigned time T_{SG};

at least one control device which is to be addressed measures an electrical parameter after the time T_{SG} which has been assigned for that at least determine control device in order to determine whether there is a downstream control device which is to be addressed; and

said at least one control device allocates itself an address if there is no downstream control device which is to be addressed.

Claim 17. (New) The method as claimed in Claim 16, wherein said electrical parameter determined is a differential voltage level at an output of the at least one control device to a downstream control device, as is obtained for determining message transmission in line with the bus system on the data bus line.

Claim 18. (New) The method as claimed in Claim 17, wherein the electrical

parameter measured is current on the data line at an output of the at least one control device to a downstream control device, when the data bus line is in the form of a single-wire data line.

Claim 19. (New) The method as claimed in Claim 16, wherein, in each particular control device, if there is a downstream control device that is to be addressed then the data bus line is closed by that particular control device, using the isolating means, and the transmission/reception unit in that particular control device is turned off.

Claim 20. (New) The method as claimed in Claim 19, wherein the isolating means comprises a switching transistor, a relay and a repeater.

Claim 21. (New) The method as claimed in Claim 20, wherein control devices which are not involved in the address allocation do not send any signals to the data bus line in the address allocation period.

Claim 22. (New) The method as claimed in Claim 21, wherein:

after a time T_{MAX}, the isolating means in the control devices which are to be addressed are closed and the latter's transmission units are turned off; and

the time T_{MAX} is chosen to be greater than any of the times T_{SG} which are individually assigned to the respective control devices which are to be addressed.

Claim 23. (New) The method as claimed in Claim 22, wherein, during address allocation the address of the control device which is to be addressed is obtained by one of:

transferring an address transmitted by a control device at the start of the address allocation period; and

incrementing an address sent by a control device at the start of an addressing cycle.

Claim 24. (New) The method as claimed in Claim 23, wherein the address allocation period is produced as part of an addressing cycle and is started repeatedly by means of automatic flow control.

Claim 25. (New) The method as claimed in Claim 24, wherein after a particular time T_{CYC} the address allocation period is restarted, with T_{CYC} being greater than T_{MAX}.

Claim 26. (New) A bus system for a plurality of control devices that are connected by a common data bus line, each of the control devices having a respective transmission/reception unit for simultaneously accessing data sent via the common data bus line, where at least one control device has isolating means for switchably interrupting the data bus line, and the at least one control device has a measuring arrangement which measures an electrical current or voltage signal on the data bus line at an output to a downstream control device, wherein

the measuring arrangement has first means for controlling the isolating means and the transmission/reception unit in the at least one control device; and

said first means takes the evaluation of the measured signals as a basis for controlling the isolating means and the transmission/reception unit.

Claim 27. (New) The bus system as claimed in Claim 26, wherein the measuring arrangement has a comparison means to which the voltage level is supplied as an input signal on the data bus line at the output of the control device, the output signal from the comparison means forming the input signal for controlling the isolating means and the transmission/reception unit.

Claim 28. (New) The bus system as claimed in Claim 27, wherein the isolating means comprises one of a switching transistor, a relay and a repeater.

Claim 29. (New) A method for assignment of addresses to a plurality of control units that are connected by a common data bus line, said method comprising:

one of said control units, acting as a master unit, transmitting a message to remaining control units, acting as slave units, via said data bus line, thereby initiating an address allocation period;

in response to said message, during said address allocation period, each of said slave units opening a switch to break said data bus line within said slave unit, and causing a dominant signal to be present at its input, which is connected to an output of a preceding slave unit;

each salve unit detecting whether a dominant signal is present at its output; and

only a slave unit which does not detect a dominant signal at its output accepting an address transmitted from the master unit at a preset time during a particular address allocation period.